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EXAMINER	
HERNANDEZ, MANUEL J	
ART UNIT	**PAPER NUMBER**
4154	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/595,908	Applicant(s) ROZEN ET AL.	
	Examiner MANUEL HERNANDEZ	Art Unit 4154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _5/18/2006_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-30_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-30_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _18 May 2006_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _5/18/2006_.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: the specification fails to comply with the guidelines as described in 37 CFR 1.77(b).

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
  (1) Field of the Invention.
  (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 12 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 1 describes “a measuring function” which is also described in dependent claim 12. It is unclear whether the measuring function refers to the described function in claim 1 or another measuring function. For examination purposes, the measuring function of claim 12 is understood to refer to the measuring function of claim 1.

5. Claim 1 describes “a measured performance” which is also described in dependent claim 18. It is unclear whether the measured performance refers to the described performance in claim 1 or another measured performance. For examination purposes, the measured performance of claim 18 is understood to refer to the measured performance of claim 1.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1-4, 6-8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (US 5,847,552) in view of Borkar et al (US 6,484,265).

Regarding claim 1, Brown teaches a device for regulating a voltage supply to a semiconductor device (Abstract), said device comprising:

a memory (Figure 2, 24) for storing a performance range (column 3, lines 23-33), wherein said performance range is associated with a respective supply voltage (column 3, lines 15-19); a measuring function for measuring a performance of said semiconductor device (column 3, lines 52-60, column 4, lines 14-18); and

a regulator (Figure 1, 16) wherein the device is characterized in that the memory stores a performance limit ("optimum operating performance", column 3, lines 33-34) of the semiconductor device and a reference circuit (Figure 2, 39) is coupled to the memory (Figure 2, 24) and is arranged to determine a lowest supply voltage (column 4, lines 55-60, column 2, lines 21-22) required to maintain a performance ("optimum operating performance", column 3, lines 33-34) of the semiconductor device at a given operational frequency (column 3, lines 56-57).

Brown fails to disclose a plurality of performance ranges, and the modification of supply voltage if a measured performance is not within a performance range.

Borkar et al teach a plurality of performance ranges (column 12, lines 29-32) and the modification of the supply voltage to said semiconductor device if a measured performance of said semiconductor device is not within a predetermined portion of said performance range associated with said voltage supplied to said semiconductor device (column 13, lines 2-6, 25-30, 35-37, column 4, lines 34-43).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Brown for regulating a voltage supply to a semiconductor device to include a plurality of performance ranges and the modification of the supply voltage if measured performance is not within a performance range as described by Borkar et al. One would have been motivated to include the plurality of performance ranges and the modification of the supply voltage to control various parameters of the semiconductor device, providing for an increase in performance, a reduced power consumption, and prevention of processor overheating. (column 1, lines 48-56, column 2, lines 1-3, column 6, lines 19-22, column 13, lines 35-37).

Regarding claim 2, Brown as modified by Borkar et al disclose a device for regulating a voltage supply to a semiconductor device as described above, but fail to disclose said performance limits stored in the memory are based on two parameters, the first parameter being current resistance drop value and the second parameter being an accuracy of the regulator.

One of ordinary skill, however, would recognize the need to take into account parameters such as the current resistance drop value and the accuracy of the regulator when setting the performance limits. For instance, if the current resistance drop value is not taken into account, then the semiconductor device would not receive sufficient voltage. If the accuracy of the regulator is not taken into account, then the semiconductor device would not receive the desired voltage.

It would have been obvious to one of ordinary skill in the art at the time of the invention to program the memory based on these two parameters. One would have been motivated to program the memory based at least on these parameters since the semiconductor device would fail to operate correctly if these two parameters were not taken into consideration at the time the memory was programmed.

Regarding claim 3, Brown as modified by Borkar et al teaches said performance range is defined to have an upper performance limit (Borkar, "THIGH," column 4, lines 20-25, column 6, lines 26-27, column 3, lines 50-57) such that if said measured performance of the semiconductor device is above said upper performance limit said regulator is arranged to reduce said voltage supplied to said semiconductor device (Borkar, column 4, lines 25-28).

Regarding claim 4, Brown as modified by Borkar et al teaches said performance range is defined to have a lower performance limit (Borkar, "TLOW," column 4, lines 28-29, column 6, lines 26-27, column 3, lines 50-57) such that if said measured performance of said semiconductor device is below said lower performance limit said

regulator is arranged to increase said voltage supplied to the semiconductor device (Borkar, column 4, lines 30-32).

Regarding claim 6, Brown as modified by Borkar et al discloses said measuring function is arranged to measure said performance of said semiconductor device by measuring said performance of a reference circuit that forms part of said semiconductor device (Brown, column 3, lines 52-60, column 4, lines 14-18).

Regarding claim 7, Brown as modified by Borkar et al disclose a device for regulating a voltage supply to a semiconductor device as described above, but fail to disclose said plurality of performance ranges are arranged to include a performance guard margin to compensate for differences between said measured performance of said reference circuit and an actual performance of a complete integrated circuit.

One of ordinary skill in the art, however, would recognize the need to compensate for differences between a measured performance of the reference circuit and the actual performance of an integrated circuit. It is well known in the art that variations exist in semiconductor devices. If the differences between said measured performance of said reference circuit and an actual performance are not taken into account, then the semiconductor device would not receive the appropriate voltage from the voltage regulator.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide a performance guard margin. One would have been motivated to include the performance guard margin to compensate for different characteristics amongst different transistors in an semiconductor device (Borkar, column 9, lines 25-29)

thereby providing means to reduce mismatches between transistors of different domains (Borkar, column 10, lines 19-42) and ultimately to control various parameters of the semiconductor device, providing for an increase in performance, a reduced power consumption, and prevention of processor overheating. (column 1, lines 48-56, column 2, lines 1-3, column 6, lines 19-22, column 13, lines 35-37).

Regarding claim 8, Brown as modified by Borkar et al discloses a ring oscillator (Brown, Figure 2, 39), wherein said measuring function measures a frequency of said ring oscillator for providing a measure of said performance of an integrated circuit (Brown, column 4, lines 14-18).

Regarding claim 9, Brown teaches a method for regulating a voltage supply to a semiconductor device (Abstract), said method comprising:

storing a performance range (column 3, lines 23-33) of the semiconductor device wherein said performance range is associated with a respective supply voltage (column 3, lines 15-19);

measuring a performance of said semiconductor device (column 3, lines 52-60, column 4, lines 14-18);

wherein the method is characterized by the step of determining a lowest supply voltage (column 4, lines 55-60, column 2, lines 21-22) required to maintain a performance (“optimum operating performance”, column 3, lines 33-34) of the semiconductor device at a given operational frequency (column 3, lines 56-57).

Brown fails to disclose a plurality of performance ranges, and the modification of supply voltage if measured performance is not within a performance range.

Borkar et al teach a plurality of performance ranges (column 12, lines 29-32) and the modification of the supply voltage to said semiconductor device if a measured performance of said semiconductor device is not within a predetermined portion of said performance range associated with said voltage supplied to said semiconductor device (column 13, lines 2-6, 25-30, 35-37, column 4, lines 34-43).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Brown for regulating a voltage supply to a semiconductor device to include a plurality of performance ranges and the modification of the supply voltage if measured performance is not within a performance range as described by Borkar et al. One would have been motivated to include the plurality of performance ranges and the modification of the supply voltage to control various parameters of the semiconductor device, providing for an increase in performance, a reduced power consumption, and prevention of processor overheating. (column 1, lines 48-56, column 2, lines 1-3, column 6, lines 19-22, column 13, lines 35-37).

9. Claims 5 and 10-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (US 5,847,552) and Borkar et al (US 6,484,265) in view of Bonnett (US 6,996,730).

Regarding claim 10, Brown and Borkar et al teach the device for regulating a voltage supply to a semiconductor device as described above but fail to disclose a plurality of process temperature compensation voltages and the modification of voltage supply with respect to a change in operational frequency.

Bonnett discloses the memory also stores a plurality of process temperature compensation voltage values, wherein said respective process temperature compensation voltage values are associated with a respective operational frequency for said semiconductor device (column 5, lines 15-22, lines 25-28), such that if said operational frequency of said semiconductor device changes to a new operational frequency, said supply voltage is modified by said regulator to substantially a same value as said process temperature compensation voltage value associated with said new operation frequency (column 2, lines 36-39).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have included the plurality of process temperature compensation voltages of Bonnett in the device for regulating a voltage supply to a semiconductor device as described by Brown and Borkar et al. One would have been motivated to modify the voltage supply regulating device as proposed to reduce the power consumption while still delivering sufficient performance (column 2, lines 16-20).

Regarding claim 5, Brown and Borkar et al as modified by Bonnett teaches said performance range is defined to have a critical lower performance limit (Bonnett, column 7, lines 56-59) such that if said measured performance of said semiconductor device is below said critical lower performance limit said regulator is arranged to increase said voltage supplied to said semiconductor device (Bonnett, column 7, lines 61-64, column 8, lines 25-29).

Regarding claim 11, Brown and Borkar et al as modified by Bonnett teaches each process temperature compensation voltage value associated with a respective

operational frequency is determined from a plurality of performance ranges stored in said memory wherein said respective performance ranges are associated with a respective supply voltage (Bonnett, column 4, Table 1).

Regarding claim 12, Brown and Borkar et al as modified by Bonnett teaches a measuring function for measuring the performance of the semiconductor device (Brown, column 3, lines 52-60, column 4, lines 14-18), wherein said regulator is arranged to modify said supply voltage to said semiconductor device if a measured performance of said semiconductor device is not within a predetermined portion of a performance range associated with said voltage supplied to the semiconductor device (Brown, column 13, lines 2-6, 25-30, 35-37, column 4, lines 34-43) for a given frequency (Bonnett, column 4, Table 1).

Regarding claim 13, Brown and Borkar et al as modified by Bonnett teaches said performance range is defined to have an upper performance limit (Borkar, "THIGH," column 4, lines 20-25, column 6, lines 26-27, column 3, lines 50-57) such that if said measured performance of said semiconductor device is above said upper performance limit said regulator is arranged to reduce said voltage supplied to said semiconductor device (Borkar, column 4, lines 30-32).

Regarding claim 14, Brown and Borkar et al as modified by Bonnett teaches said performance range is defined to have a lower performance limit (Borkar, "TLOW," column 4, lines 28-29, column 6, lines 26-27, column 3, lines 50-57) such that if said measured performance of said semiconductor device is below said lower performance

limit said regulator is arranged to increase said voltage supplied to said semiconductor device (Borkar, column 4, lines 30-32).

Regarding claim 15, Brown and Borkar et al as modified by Bonnett teaches said performance range is defined to have a critical lower performance limit (Bonnett, column 7, lines 56-59) such that if said measured performance of said semiconductor device is below said critical lower performance limit said regulator is arranged to increase said voltage supplied to said semiconductor device (Bonnett, column 7, lines 61-64, column 8, lines 25-29).

Regarding claim 16, Brown and Borkar et al as modified by Bonnett teaches said measuring function is arranged to measure the performance of said semiconductor device by measuring said performance of a reference circuit that forms part of said semiconductor device (Brown, column 3, lines 52-60, column 4, lines 14-18).

Regarding claim 17, Brown, Borkar et al and Bonnett teach a device for regulating a voltage supply to a semiconductor device as described above, but fail to disclose said plurality of performance ranges are arranged to include a performance guard margin to compensate for differences between said measured performance of said reference circuit and an actual performance of said semiconductor device.

One of ordinary skill in the art, however, would recognize the need to compensate for differences between a measured performance of the reference circuit and the actual performance of an integrated circuit. It is well known in the art that variations exist in semiconductor devices. If the differences between said measured performance of said reference circuit and an actual performance are not taken into

account, then the semiconductor device would not receive the appropriate voltage from the voltage regulator.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide a performance guard margin. One would have been motivated to include the performance guard margin to compensate for different characteristics amongst different transistors in an semiconductor device (Borkar, column 9, lines 25-29) thereby providing means to reduce mismatches between transistors of different domains (Borkar, column 10, lines 19-42) and ultimately to control various parameters of the semiconductor device, including performance, power consumption, and temperature (Borkar, column 2, lines 1-3, column 6, lines 19-22, column 13, lines 35-37).

Regarding claim 18, Brown and Borkar et al as modified by Bonnett teaches a ring oscillator (Brown, Figure 2, 39), wherein said measuring function measures a frequency of said ring oscillator for providing a measure of a performance of the semiconductor device (Brown, column 4, lines 14-18).

Regarding claim 19, Brown and Borkar et al teach a method for regulating a voltage supply to a semiconductor device as described above, but fail to disclose a plurality of process temperature compensation voltages and the modification of voltage supply with respect to a change in operational frequency.

Bonnet discloses said set of storing comprises storing a plurality of process temperature compensation voltage values, wherein respective process temperature

compensation voltage values are associated with a respective operational frequency for said semiconductor device (column 5, lines 15-22, lines 25-28); and

said step of modifying comprises modifying a supply voltage to said semiconductor device if an operational frequency of said semiconductor device changes to a new operational frequency, wherein said supply voltage is modified to substantially a same value as a process temperature compensation voltage value associated with said new operational frequency (column 2, lines 36-39).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have included the plurality of process temperature compensation voltages of Bonnett in the device for regulating a voltage supply to a semiconductor device as described by Brown and Borkar et al. One would have been motivated to modify the voltage supply regulating device as proposed to reduce the power consumption while still delivering sufficient performance (column 2, lines 16-20).

10. Claims 20, 21 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (US 5,847,552) in view of Bonnett (US 6,996,730).

Regarding claim 20, Brown discloses a device for regulating a voltage supply to a semiconductor device (Abstract), wherein the device is characterized in that the memory stores a performance limit (Brown, "optimum operating performance", column 3, lines 33-34) of the semiconductor device and a reference circuit (Brown, Figure 2, 39) is coupled to the memory (Brown, Figure 2, 24) and is arranged to determine a lowest supply voltage (Brown, column 4, lines 55-60, column 2, lines 21-22) required to maintain a performance (Brown, "optimum operating performance", column 3, lines 33-

34) of the semiconductor device at a given operational frequency (Brown, column 3, lines 56-57).

Brown fails to disclose a plurality of process temperature compensation voltage values and the modification of voltage supply with respect to a change in operational frequency.

Bonnett discloses a memory for storing a plurality of process temperature compensation voltage values, wherein said respective process temperature compensation voltage values are associated with a respective operational frequency for said semiconductor device (Bonnett, column 5, lines 15-22, lines 25-28); and a regulator for modifying said supply voltage to said semiconductor device if said operational frequency of said semiconductor device changes to a new operational frequency (Bonnett, column 2, lines 36-39), and modify said supply voltage to substantially a same value as said process temperature compensation voltage value associated with said new operational frequency (Bonnett, column 2, lines 36-39).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have included the plurality of process temperature compensation voltages of Bonnett in the device for regulating a voltage supply to a semiconductor device as described by Brown. One would have been motivated to modify the voltage supply regulating device as proposed to reduce the power consumption while still delivering sufficient performance (column 2, lines 16-20).

Regarding claim 21, Brown and Bonnett teach a device for regulating a voltage supply to a semiconductor device as described above, but fail to disclose said

performance limit stored in the memory is based on a current resistance drop value and an accuracy of the regulator.

One of ordinary skill, however, would recognize the need to take into account parameters such as the current resistance drop value and the accuracy of the regulator when setting the performance limits. For instance, if the current resistance drop value is not taken into account, then the semiconductor device would not receive sufficient voltage. If the accuracy of the regulator is not taken into account, then the semiconductor device would not receive the desired voltage.

It would have been obvious to one of ordinary skill in the art at the time of the invention to program the memory based on these two parameters. One would have been motivated to program the memory based at least on these parameters since the semiconductor device would fail to operate correctly if these two parameters were not taken into consideration at the time the memory was programmed.

Regarding claim 30, Brown discloses a method for regulating a voltage supply to a semiconductor device (Brown, abstract), said method characterized by the step of determining a lowest supply voltage (Brown, column 4, lines 55-60, column 2, lines 21-22) required to maintain a performance (Brown, “optimum operating performance”, column 3, lines 33-34) of the semiconductor device at a given operational frequency (Brown, column 3, lines 56-57)

Brown fails to disclose a plurality of process temperature compensation voltages and the modification of voltage supply with respect to a change in operational frequency.

Bonnett discloses storing a plurality of process temperature compensation voltage values, wherein respective process temperature compensation voltage values are associated with a respective operational frequency for said semiconductor device (Bonnett, column 5, lines 15-22, lines 25-28); and modifying a supply voltage to said semiconductor device if an operational frequency of said semiconductor device changes to a new operational frequency (Bonnett, column 2, lines 36-39), and modifying said supply voltage to substantially a same value as a process temperature compensation voltage value associated with said new operational frequency (Bonnett, column 2, lines 36-39).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have included the plurality of process temperature compensation voltages of Bonnett in the device for regulating a voltage supply to a semiconductor device as described by Brown. One would have been motivated to modify the voltage supply regulating device as proposed to reduce the power consumption while still delivering sufficient performance (column 2, lines 16-20).

11. Claims 22-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (US 5,847,552) and Bonnett (US 6,996,730) in view of Borkar et al (US 6,484,265).

Regarding claim 22, Brown and Bonnett teach the device for regulating a voltage supply to a semiconductor device as described above but fail to disclose a plurality of performance ranges.

Borkar et al disclose each process temperature compensation voltage value associated with a respective operational frequency is determined from a plurality of performance ranges (Borkar, column 12, lines 29-32) stored in said memory wherein said respective performance ranges are associated with a respective supply voltage (Borkar, column 12, lines 29-32).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Brown and Bonnett for regulating a voltage supply to a semiconductor device to include a plurality of performance as described by Borkar et al. One would have been motivated to include the plurality of performance ranges to facilitate control of various parameters of the semiconductor device, including performance, power consumption, and temperature (column 2, lines 1-3, column 6, lines 19-22, column 13, lines 35-37).

Regarding claim 23, Brown and Bonnett as modified by Borkar et al teach a measuring function for measuring the performance of the semiconductor device (Borkar, column 10, lines 51-53, 34-66), wherein said regulator is arranged to modify said supply voltage to said semiconductor device if a measured performance of the semiconductor device is not within a predetermined portion of a performance range associated with said voltage supplied to said semiconductor device (Borkar, column 13, lines 2-6, 25-30, 35-37, column 4, lines 34-43) for a given frequency (Borkar, column 4, lines 53-56).

Regarding claim 24, Brown and Bonnett as modified by Borkar et al teach said performance range is defined to have an upper performance limit (Borkar, "THIGH," column 4, lines 20-25, column 6, lines 26-27, column 3, lines 50-57) such that if said

measured performance of said semiconductor device is above said upper performance limit said regulator is arranged to reduce said voltage supplied to said semiconductor device (Borkar, column 4, lines 25-28).

Regarding claim 25, Brown and Bonnett as modified by Borkar et al teach said performance range is defined to have a lower performance limit (Borkar, "TLOW," column 4, lines 28-29, column 6, lines 26-27, column 3, lines 50-57) such that if said measured performance of said semiconductor device is below said lower performance limit said regulator is arranged to increase said voltage supplied to said semiconductor device (Borkar, column 4, lines 30-32).

Regarding claim 26, Brown and Bonnett as modified by Borkar et al teach said performance range is defined to have a critical lower performance limit (Bonnett, column 7, lines 56-59) such that if said measured performance of said semiconductor device is below said critical lower performance limit said regulator is arranged to increase said voltage supplied to said semiconductor device (Bonnett, column 7, lines 61-64, column 8, lines 25-29).

Regarding claim 27, Brown and Bonnett as modified by Borkar et al discloses said measuring function is arranged to measure the performance of said semiconductor device by measuring said performance of a reference circuit that forms part of said semiconductor device (Brown, column 3, lines 52-60, column 4, lines 14-18).

Regarding claim 28, Brown, Bonnett, and Borkar et al teach the device for regulating a voltage supply to a semiconductor device as described above but fail to disclose said plurality of performance ranges are arranged to include a performance

guard margin to compensate for differences between said measured performance of said reference circuit and an actual performance of said semiconductor device.

One of ordinary skill in the art, however, would recognize the need to compensate for differences between a measured performance of the reference circuit and the actual performance of an integrated circuit. It is well known in the art that variations exist in semiconductor devices. If the differences between said measured performance of said reference circuit and an actual performance are not taken into account, then the semiconductor device would not receive the appropriate voltage from the voltage regulator.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide a performance guard margin. One would have been motivated to include the performance guard margin to compensate for different characteristics amongst different transistors in an semiconductor device (Borkar, column 9, lines 25-29) thereby providing means to reduce mismatches between transistors of different domains (Borkar, column 10, lines 19-42) and ultimately to control various parameters of the semiconductor device, including performance, power consumption, and temperature (Borkar, column 2, lines 1-3, column 6, lines 19-22, column 13, lines 35-37).

Regarding claim 29, Brown and Bonnett as modified by Borkar et al discloses a ring oscillator (Brown, Figure 2, 39), wherein said measuring function measures a frequency of said ring oscillator for providing a measure of a performance of the semiconductor device (Brown, column 4, lines 14-18).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Morales (US 7,075,276) is cited to show a ring oscillator and measuring function utilized to compensate for variations in an integrated circuit. Schutz et al (US 5,440,520), Afek et al (5,712,589), and Clark et al (US 6,664,775) are cited to show relevant devices for regulating a voltage supply to a semiconductor device.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MANUEL HERNANDEZ whose telephone number is (571)270-7916. The examiner can normally be reached on 5/4/9 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seungsook Ham can be reached on 571-272-2405. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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MH

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Primary Examiner